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Efficient Inverter Configuration for Hybrid Electric Vehicles: A Three Phase Integrated Approach

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Abstract: Multilevel inverters (MLIs) have become essential in power electronics due to their capability to improve power quality, minimize harmonic distortion and enhance efficiency in medium and HV applications. It achieves a smoother waveform, reducing total harmonic distortion (THD). Hybrid electric vehicles (HEVs) are increasingly recognized for their ability to reduce fuel consumption and emissions in modern transportation. Their performance largely depends on the efficiency of power conversion systems, particularly in the inverter setup. In this study, a novel 3-phase 25-level MLI configuration is proposed with fewer switches. The primary objective is to reduce harmonics through high-level MLI implementation and motor optimization in electric vehicle applications. Proposed research suggests a novel three phase 25-level hybrid inverter tailored for hybrid electric vehicles, featuring an innovative hybrid DC-DC and DC-AC topology that utilizes fewer switches to enhance cost effectiveness. Simulation results indicate that the three phase 25-level MLI improves voltage stability and further mitigates harmonics compared to a single phase configuration. While comparing with conventional converters, MLIs offer significant benefits, including high frequency switching and advanced modulation techniques for precise control. It generates output voltage with minimal harmonics, lower dv/dt stress on switches and introduces common mode voltage. In particular, the 3-phase 25-level inverter system achieves a smoother waveform, reducing THD. The proposed system has been validated using MATLAB/Simulink. Additionally, the comparative analysis between the proposed 1-ph, and 3-ph 25-level MLI topologies are also presented.

Keywords: Multilevel Inverter, Hybrid Electric Vehicles, Pulse Width Modulation, Phase Disposition.

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1. Introduction

Power electronics has emerged as one of the most actively researched and rapidly evolving domains within electrical engineering. The scope of power electronics continues to expand, especially in solar photovoltaic systems, which are becoming increasingly essential in the modern energy landscape. With the rising demand for uninterrupted, high-quality power and the rapid depletion of non-renewable energy sources, engineers in the field are driven to develop innovative solutions. One significant area of study in power electronics is multilevel inverters [1] (Voltage Source Converters). These inverters have garnered considerable attention for industrial medium voltage applications. However, as the number of voltage levels in conventional MLIs

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increases, the complexity [2] of both the power and control circuits escalates due to enhancing number of components and driving circuits. Additionally, system reliability tends to decrease while the number of discrete elements increases. To enhance efficiency and refine output voltage waveforms, various MLI topologies have been introduced [3]. Multilevel inverters have become crucial in modern applications, particularly with the increasing integration of Renewable Energy Sources (RES) [4 - 5]. They are widely used in micro grid systems and are particularly advantageous for medium and high-power applications [6]. Traditionally, inverters were limited to two voltage levels (+V and –V), regulated through Pulse Width Modulation (PWM) techniques [7]. However, this methodology is skilled at addressing issues such as prominent harmonic distortion, Electro Magnetic Interference (EMI), and dv/dt stress [8]. The foremost concern is the high THD and reducing semiconductor related switches [9] to mid level and high voltage grids (2.3, 3.3, 4.16, or 6.9 kV). To discuss these limitations, the perception of MLI was presented. By utilizing multiple voltage levels, MLI not only effectively diminishes the harmonic distortion [10] but also generates a smooth sinusoidal output waveform and distributes the voltage stress more efficiently across power electronic switches [11 - 12]. So, these devices become gradually imperative in industrial applications, like static VAR compensators, renewable energy systems and motor drives [13]. Over the last few years, numerous MLI topologies have been established. This indicates remarkable encroachment in the field of PE and involves a variety of configurations, including H-Bridge Multilevel Inverters (CHB-MLI), Flying Capacitor Multilevel Inverters (FC-MLI) [14], Diode Clamped Multilevel Inverters (DC-MLI) and Cascaded [15 - 16]. Each of these devices utilizes independent DC sources, contributing to their operational flexibility. With multiple voltage levels via a considerate integration of ideal power switches, capacitors and diodes, these innovative topologies are designed to generate stepped waveforms [17]. In the evolution of MLI technology, the 3-level designs, described by voltage levels of (0, $+V_{dc,}$ and $-V_{dc}$) have been a noteworthy step forward. MLIs facilitate the creation of a more refined staircase waveform [18 - 19], which positively impacts the quality of the power output by incorporating more voltage levels. This upgrading topology assists in reducing THD, which is a crucial metric for maintaining the efficiency and longevity of the systems and diminishes dv/dt stress [20], which is a rapid voltage change. Such reductions enhance the reliability and performance of the inverter, leading to a more efficient and effective power conversion. As voltage levels increase, complexity is encountered in switching control and voltage imbalance [21 - 22]. To mitigate these issues, advanced control techniques, optimized driver circuits and efficient modulation approaches are required. Cascaded Hybrid MLIs equipped with isolated DC voltage sources are very dominant among the other topologies [23] due to their ability to operate without the need for capacitors and diode clamping. By increasing the number of H-bridges, it is possible to enhance the voltage levels that produce a smooth sinusoidal waveform [24 - 25]. However, increased control complexity is the substantial drawback, due to of more number of power electronic switches required, regardless of their efficiency Though, these MLI topology having significant advantages for instance, usages fewer components [26] achieving the same number of voltage levels while compared to conventional multilevel converters, eliminates the need for clamping-diodes and voltage balancing-capacitors [27 - 28] provisions soft-switching techniques, reducing reliance on bulky and less efficient resistor capacitor diode snubber circuits, it is suffering from a drawback, the requirement of separate DC voltage sources [29] for real power conversion, which may restrict certain applications. The present study addresses a novel 3-phase 25- level MLI topology that lessens the number of switches while keeping the output voltage levels high. This design also has low THD and high efficiency, which makes it perfect for electric vehicles (EVs) motor drive applications like PMSM and BLDC systems [30]. The significant contributions of this work include:

- Optimization of the number of switching-components and DC-sources this design effectively
- Minimization of system complexity while maintaining superior out-put voltage quality with reduced THD.
- Optimization of voltage stress distribution and power conversion efficiency.

A comparative evaluation demonstrating the proposed topology achieves design optimally balances component count, voltage stress, conversion efficiency, harmonic distortion and maximizes performance and the same or better efficiency than other designs. As per prior research, the main objective of this paper is to deliver a higher-level output voltage with less control complexity and lower THD. Section 2 outlines the hybrid electric vehicles, Section 3 illustrates the dynamic modeling and control of converter configuration, Section 4 includes phase disposition in multi carrier PWM, Section 5 presents Single phase 25 - level MLI topology, Section 6 describes the simulation of the proposed 3-phase, 25-level MLI configuration and results discussion & conclusion are described in Section 7.

2. Hybrid electric vehicles

The following Fig. 1, illustrates the schematic example of HEV. This system comprises four key components, electric motor, a generator, a battery management system and DC/DC converter topology. Each component plays a vital role in overall functionality. It effortlessly manages and coordinates the driving forces generated via the ICE, electric motor and generator by leveraging a planetary gear system. To ensure smooth transitions, optimize vehicle performance between propulsion sources and improve overall efficiency, this collaboration is crucial. A 57 kW, gasoline engine operating at 6000 RPM, the ICE subsystem configuration is designed for high-performance output. The engine maintains stability by regulating speed and preventing overshooting, equipped with a speed governor. Along with the vehicle dynamic subsystem integrates all mechanical components such as chassis, suspension, wheels, and steering system. A 57 kW, gasoline engine operating at 6000 RPM, the ICE subsystem configuration is designed for high performance output. The engine maintains stability by regulating speed and preventing overshooting, equipped with a speed governor. Along with the vehicle dynamic subsystem, which integrates all mechanical components such as chassis, suspension, wheels, and steering system.

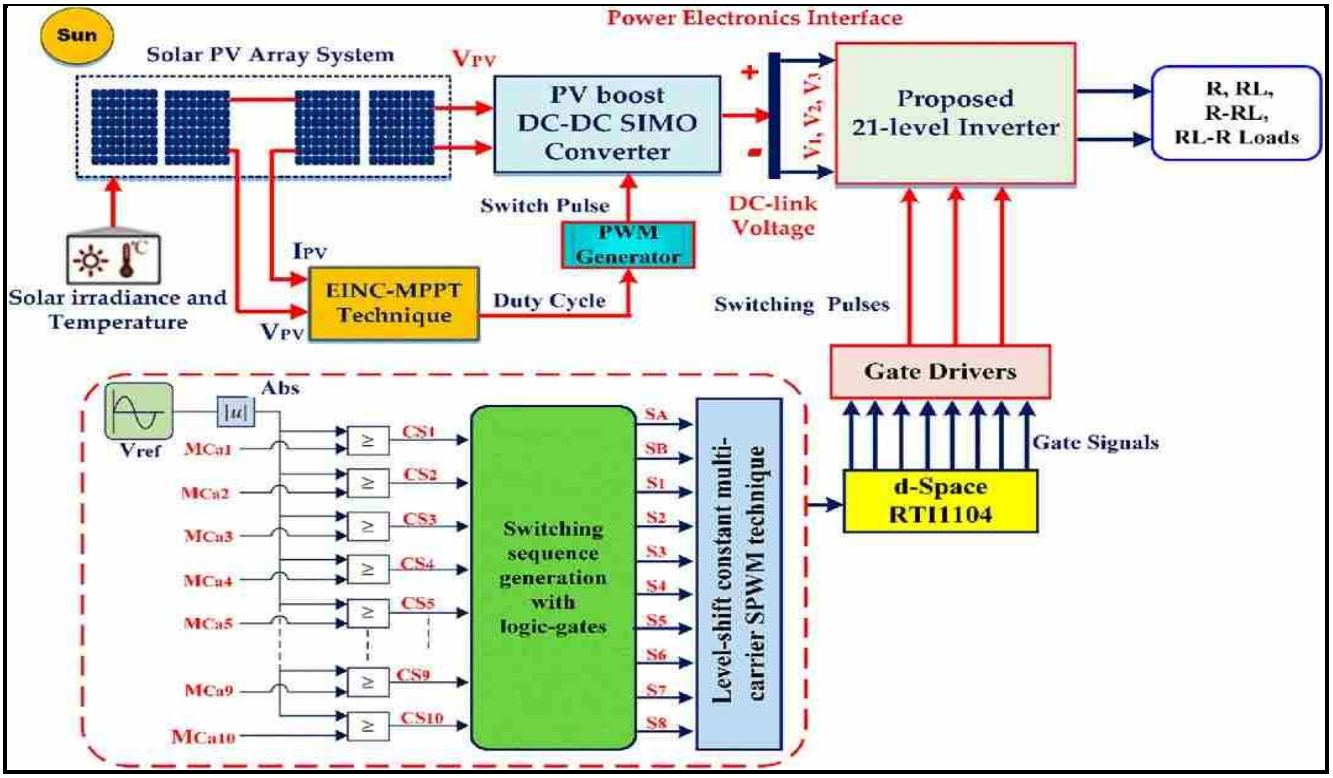

Fig. 1: Schematic exemplary of HEV

All of these play a key role in vehicle handling, stability and driving comfort. An additional essential subsystem is the Energy Management Subsystem (EMS), which adapts to dynamic driving conditions and energy demands. This is responsible for producing precise reference signals to coordinate the motor drive, generator and ICE operation. Also, the EMS subsystem monitors and optimizes energy flow in order to improve both efficiency and longevity of the vehicle's electrical systems. The chief parts of the system are batteries, motors and inverters, which transform DC from the battery into AC to drive the motor. Furthermore, in gathering and processing data, optimizing vehicle performance and safety sensors play a decisive role in the system. In modelling, the design and integration of key components in electric vehicles, the choice between a 400 Volt and 800 Volt battery systems plays a crucial role. By carefully selecting and strategically arranging these components, efficient EVs can align with sustainability intentions and evolving consumer demands. Here, two conversions take place viz DC/DC and DC/AC.

3. Dynamic modeling and control of DC/DC & DC/AC converter configuration

3.1 DC/DC modeling

Transformer less inverters need a voltage boost stage when processing power from low-voltage sources to keep the DC bus voltage at a suitable level for transferring power to the load or grid. This challenge can be addressed with a configuration where the necessary voltage step-up is achieved using a 2-stage converter, which contains a DC/DC boost converter followed by a voltage source inverter (VSI). Numerous articles discuss various DC/DC converters suitable for renewable energy applications, with most topologies exhibiting voltage source features in their outputs. While this feature can lessen the output voltage ripple when feeding linear loads, it needs an additional inductor for cases where the converter shoots up current into the utility grid. Moreover, the shoot-up current cannot be pre-controlled by the DC/DC converter, causing the DC/AC stage that links the converter to the grid to switch at high frequencies, thereby growing overall system losses. Thus, the DC/DC boost buck converter emerges as a robust power converter for these applications. This topology combines the boost and buck structures into a non-isolated, bidirectional, step-up/step-down DC-DC converter with high power density and continuous I/P and O/P currents. Additionally, it is a multipurpose converter suitable for various applications, including PV systems, high efficiency wireless power transfer, AC power generation, PF correction and thermoelectric generators. Furthermore, it can be modified for multilevel and 3-phase applications. The schematic of the DC-DC configuration for HEV is depicted in Fig. 2.

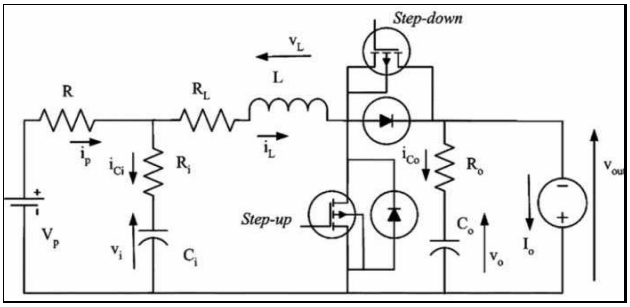

Fig. 2: DC-DC configuration

DC-DC power converter at no losses (ideal case) (1-2)

$$w_{dc\_in} = v_{in}.i_{in} \quad (1)$$

$$w_{dc\_out} = v_{out}.i_{out} \quad (2)$$

Power at the intermediate DC link as in eq (3),

$$w_{dc\_out}^{dc-dc} = w_{in}^{invt} + w_{loss} \quad (3)$$

$w_{dc_{out}}^{dc-dc}$ = Power output of DC − DC power converter
w_{in}^{invt} = Inverter input of DC − DC power converter
w_{loss} = Power loss at DC − DC power converter

By considering dynamic storage, (4)

$$c_{link}.v_{dc}\frac{dv_{dc}}{dt} = w_{dc\_out}^{dc-dc} - w_{in}^{invt} \quad (4)$$

Converter output power is (5),

$$w_{dc\_out} = \eta_{dc-dc}.w_{dc\_in} = v_{dc}.i_{dc} \quad (5)$$

c_{link} = Capacitor link
v_{dc} = DC voltage
i_{dc} = DC current

Fig. 3, depicts the input voltage waveform of DC/DC converter, whereas Fig. 4 and Fig. 5, depicts its output voltage and current waveform respectively. Modern PE heavily relies on DC/AC converters, as they enable the transformation of DC sources into AC essential for most electrical applications.

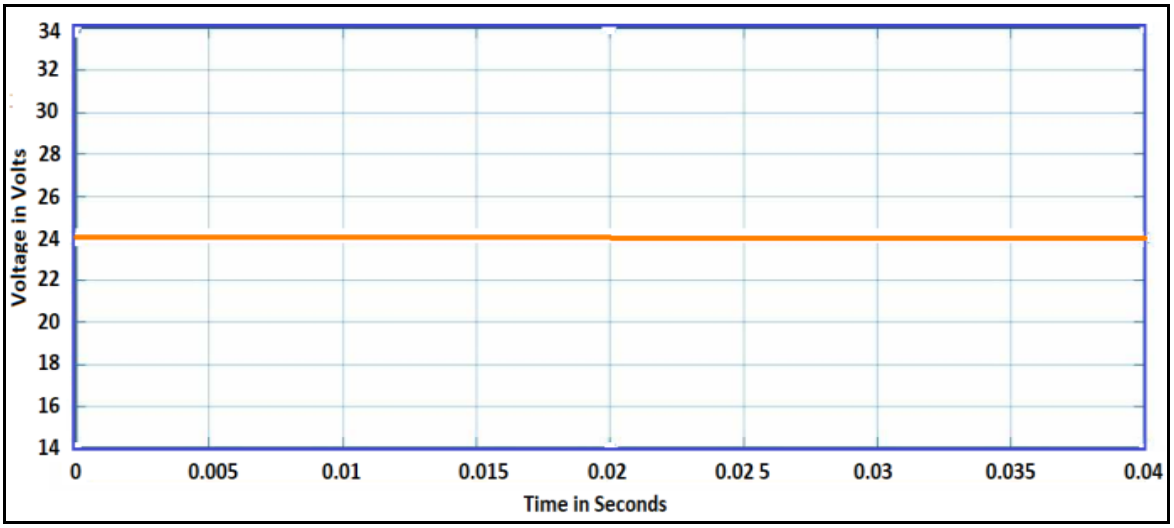

Fig. 3: Input voltage waveform of DC/DC converter.

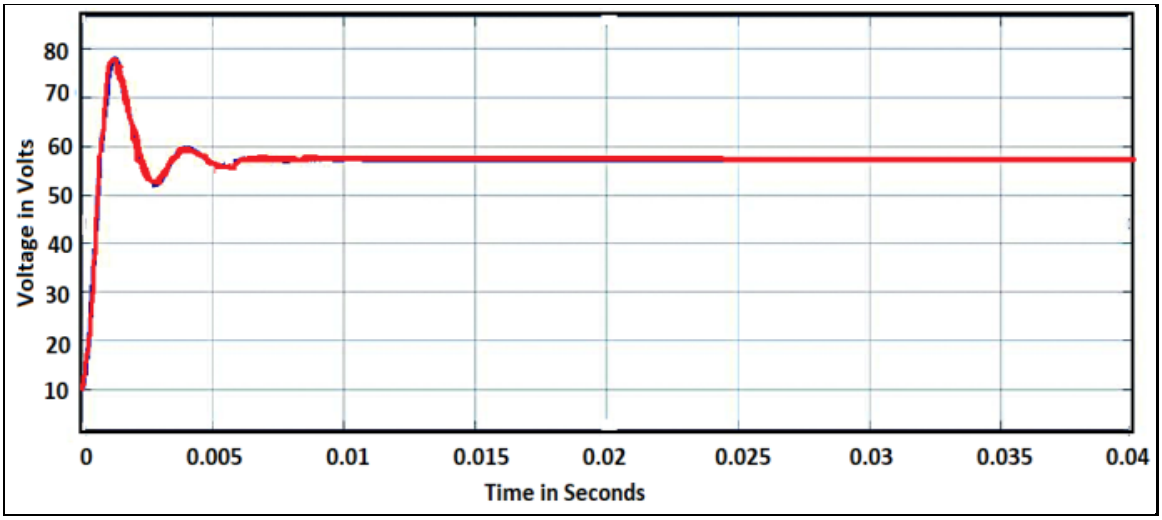

Fig. 4: Output voltage waveform of DC/DC converter.

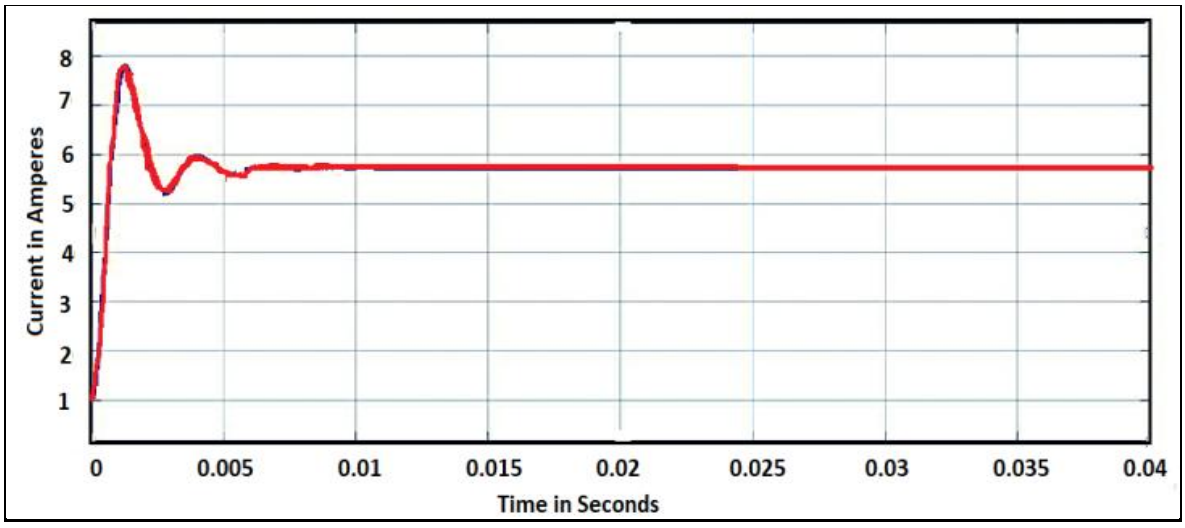

Fig. 5: Output current waveform of DC-DC converter.

3.2 DC/AC modeling

These converters play a critical role in several domains, including motor drives, uninterruptible power supplies (UPS), EVs and renewable energy systems. It also covers the key components such as circuit topologies and operational modes. There are two key types of inverters, viz. Voltage Sourced Inverters (VSI) and Current Sourced Inverters (CSI). VSIs generate the desired AC output voltage waveform while upholding a constant input DC voltage. Whereas CSIs produce the desired AC output current waveform using a persistent input current. Since both VSI and CSI are duals, their functionalities can be understood by comparing their respective voltage and current dualities. The Fig. 6 depicts the operating model of inverter configurations for electric vehicles.

The Input DC power to the inverter in DC-AC Converter (Inverter) is given by (6),

$$w_{in}^{invt} = v_{dc} . i_{dc} \quad (6)$$

Where,
$w_{in}^{invt} = Inverter\ input (DC - AC\ conevrter)$
For a balanced three phase, the output AC power (7),

$$w_{ac} = \frac{3}{2}(v_d i_d + v_q i_q) \quad (7)$$

$w_{ac} = AC\ power\ output$
$v_d = direct\ axis\ voltage$
$i_d = direct\ axis\ current$
$v_q = quadrature\ \ axis\ voltage$
$i_q = \ quadrature\ \ axis\ current$
Converter output power, for a 3-phase inverter, the L-to-L output voltage (fundamental component) is given by (8),

$$w_{ac\_out} = \eta_{dc-ac} . w_{invt\_in} = \sqrt{3} v_{LL} . i_L \cos(\phi) \quad (8)$$

Where
$\eta_{dc-ac} = Inverter\ efficiency$
$v_{LL} = Line - to - line\ voltage$
$i_L = line\ current$
$\cos(\phi) = \ Power\ factor$

Then the total power flow (Collaborative System Equation (9))

$$w_{total} = \eta_{dc-ac} . \eta_{dc-ac} . w_{dc\_in} = \eta_{in} . w_{dc\_in} \quad (9)$$

This is the core collaborative equation, showing how input DC power is converted efficiently into motor-driving AC power. For an HEV, the DC/DC converter and DC/AC converter (inverter) work together to manage and convert power from the battery (source) to drive the AC load and vice versa during regenerative braking.
Where,

$\eta_{dc-ac} = efficiency\ of\ the\ DC - AC\ coverter$

This provides the intermediate high-voltage DC for the inverter.

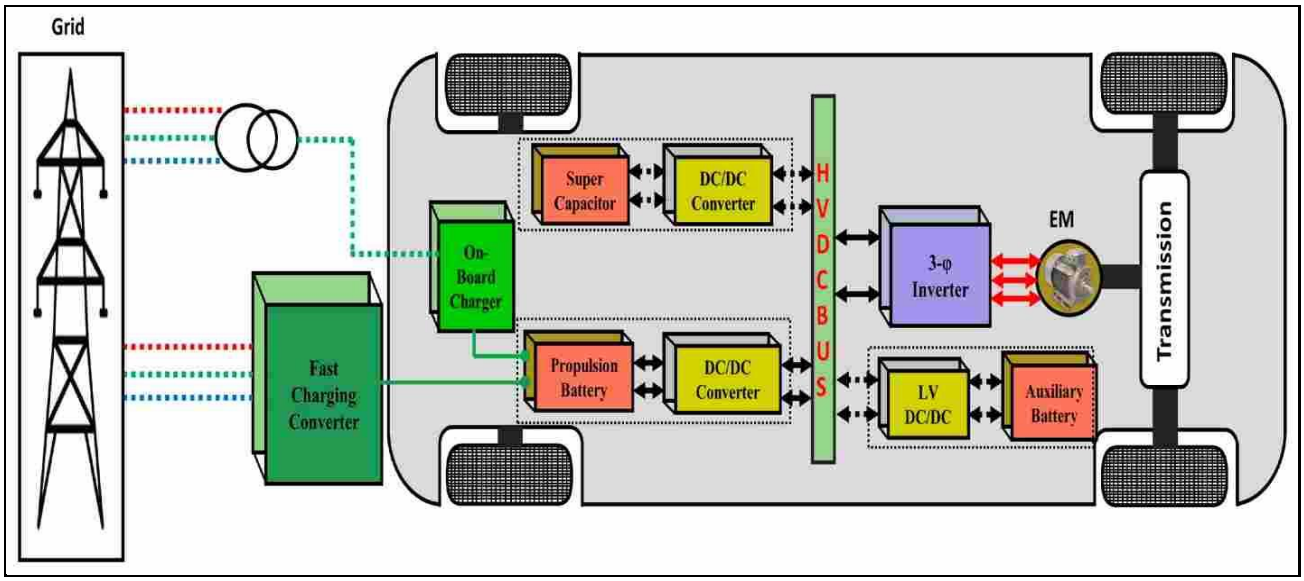

Fig. 6: EV configuration with inverter topology.

4. Phase disposition (PD) in multi-carrier PWM

Phase Disposition (PD) is a widely used Multi Carrier Pulse Width Modulation (MCPWM) technique designed for controlling MLIs. Its primary objective is to generate a smooth AC output waveform while significantly reducing harmonic distortion. In PD-PWM, multiple high frequency triangular carrier signals are employed. At the starting all of these remain coordinated and maintain alignment throughout the modulation process at the same point. A low frequency sine wave serves as the reference signal, which is unceasingly compared with the carrier signals.

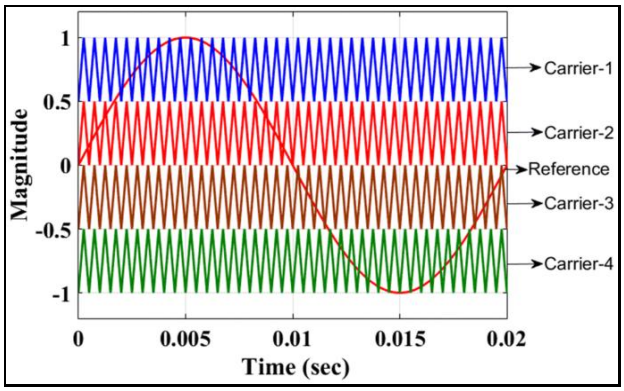

Fig. 7: Phase disposition in Multi Carrier PWM

The switches of the inverter are triggered based on whether the reference falls below each carrier or the signal surpasses. The output waveform that closely resembles a pure sine wave; this progression results in the generation of multiple voltage levels. Synchronization of all carriers ensures a more balanced waveform with minimal harmonic distortion, improves waveform smoothness and symmetry for more efficient power conversion (improved output voltage quality) are key advantage of this technique. PD-PWM is widely adopted in industrial applications and is easier to implement when compared with alternative PWM techniques such as Phase-Opposition Disposition (POD) and Alternative-Phase Opposition Disposition (APOD). The Fig. 7, depicts the Phase Disposition (PD) in Multi-Carrier PWM, used for generating gate pulses for the proposed 25-level MLI topology.

5. Single phase 25- level MLI topology

Single phase 25- level MLI configuration utilizes four distinct, unequal DC sources and 12 switches to achieve output voltage ranging from +12 V_{dc} to -12 V_{dc} successfully. Fig. 8, represents the MATLAB/Simulink model of the proposed 1- phase 25-level MLI. This configuration significantly optimizes efficiency by minimizing DC sources by 67% and reducing the number of switches by 75%. Table. 1, summarizes the necessary switching patterns for generating the required 25-level output voltage. To mitigate THD and enhance the performance, various PWM techniques are employed in multilayer inverters. Numerous multicarrier PWM methods are available to improve waveform quality. This study specifically implements an MCPWM strategy with PD, effectively reducing THD in both output voltage and current. As the number of levels increases, the complexity of the power and control circuits in typical MLIs also tends to rise, owing to the increased number of driving circuits and other constituents involved. This increase in discrete components may impact system reliability. To address these challenges, various MLI topologies have been thoughtfully developed to enhance component efficiency while simultaneously improving the output voltage waveform. Recent research efforts in this area have explored techniques for fine-tuning triggering angles, which can aid in minimizing the generated harmonics during the operation as well as reducing the overall number of required switches. The calculation of typical cascaded-MLI circuit's switching devices and DC sources can be approached as (10 – 11).

$$\text{Switch count} = 2(\text{Level} - 1) \quad (10)$$

$$\text{DC Source count} = (\text{Level} - 1)/2 \quad (11)$$

For a single-phase 25-level inverter, the switching table typically lists the states of switches corresponding to each voltage level. Since the same switching logic is applied to the other two phases with a 120° phase shift, the table remains consistent across phases, with appropriate phase offsets. In the recommended configuration, the number of switching devices and DC sources are chosen as (12 - 13),

$$\text{Switch count} = (\text{Level} - 1)/2 \quad (12)$$

$$\text{DC Source count} = (\text{Level} - 1)/6 \quad (13)$$

Number of H-bridge cells per phase required (14),

$$m = 2N + 1 \quad (14)$$

Where,
m is the number of voltage level
N is the number of H-bridge cells per phase
For 25 levels, N = 12

Total output voltage is (15),

$$v_{out}(t) = \sum_{i=1}^{12} v_i(t) \quad (15)$$

Where, $v_i(t) \in \{-v_{dc}, 0, +v_{dc}\}$

It gives level from is $-12v_{dc}$ to $+12v_{dc}$ which includes 25 discrete steps.

$$-12v_{dc}, -121v_{dc}, -10v_{dc} \dots \dots\ 0 \dots . . +10v_{dc}, +11v_{dc}, +12v_{dc}\}$$

Total output voltage in fourier series form (16),

$$v_{out}(\omega t) = \sum_{n=1,3.5\dots}^{\infty} \left(\frac{4v_{dc}}{n\pi} \sum_{k=1}^{12} \cos(n\theta_k)\right) \sin(\omega t) \quad (16)$$

Where,
n = *odd harmonic number*
θ_k= switching angle of kth cell (for positive half cycle)

By solving this to eliminate lower order harmonics like 5th, 7th, 9th, 11th etc., by maintaining the fundamental.
Modulation index (17),

$$m_a = \frac{v_{ref}}{12v_{dc}} \quad (17)$$

Where
v_{ref} = Desired fundamental voltage peak of the output fundamental component.

This topology operates based on a modular cascaded architecture, wherein each inverter cell is supplied by independent DC sources (*VDC*$_1$–*VDC*$_4$) to collectively synthesize a multilevel output voltage waveform. The power switches (Q_1–Q_4 and S_1–S_8) are driven in a precisely coordinated switching sequence to establish distinct conduction paths, as illustrated in the operating modes shown in the Fig. 9 (a), (b), (c) & (d). In each mode, selected switches are turned ON to either insert or bypass specific DC sources, resulting in the generation of multiple discrete voltage levels at the load terminals.

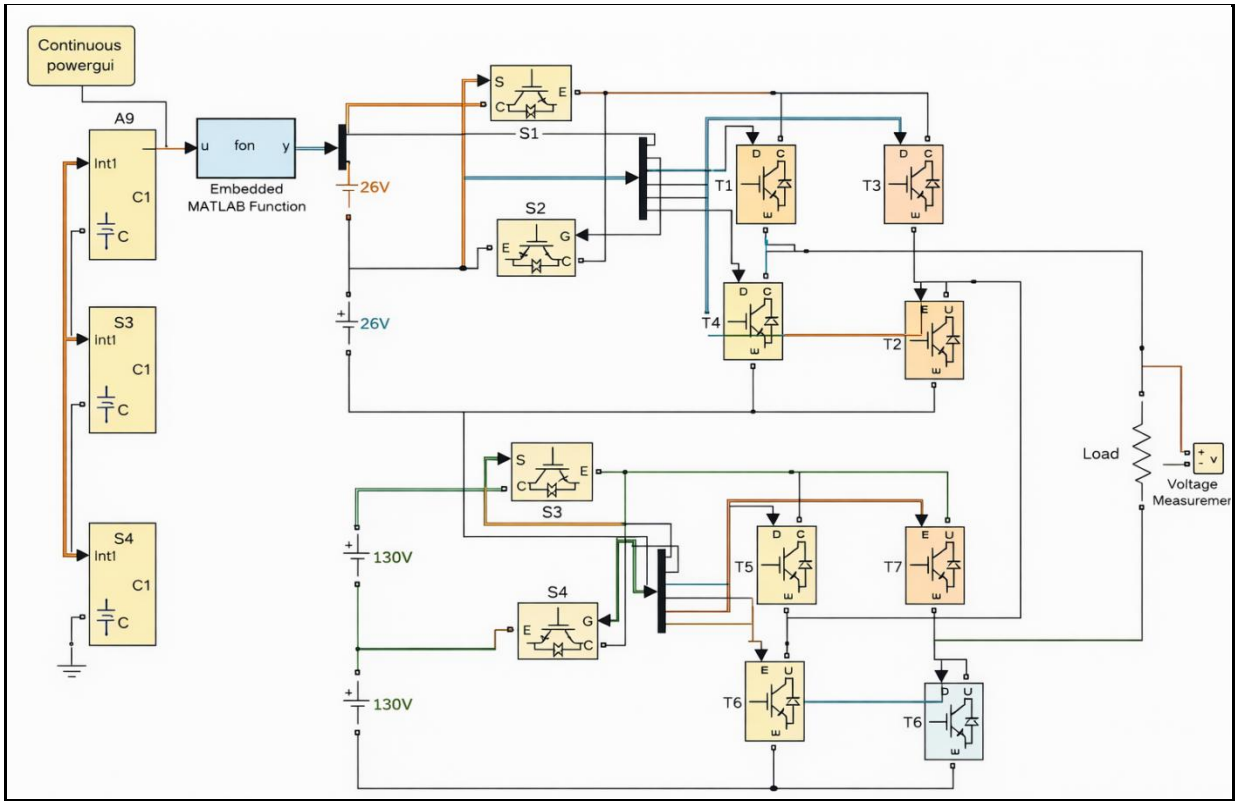

Fig. 8: Single phase 25 level inverter using sub multilevel cells.

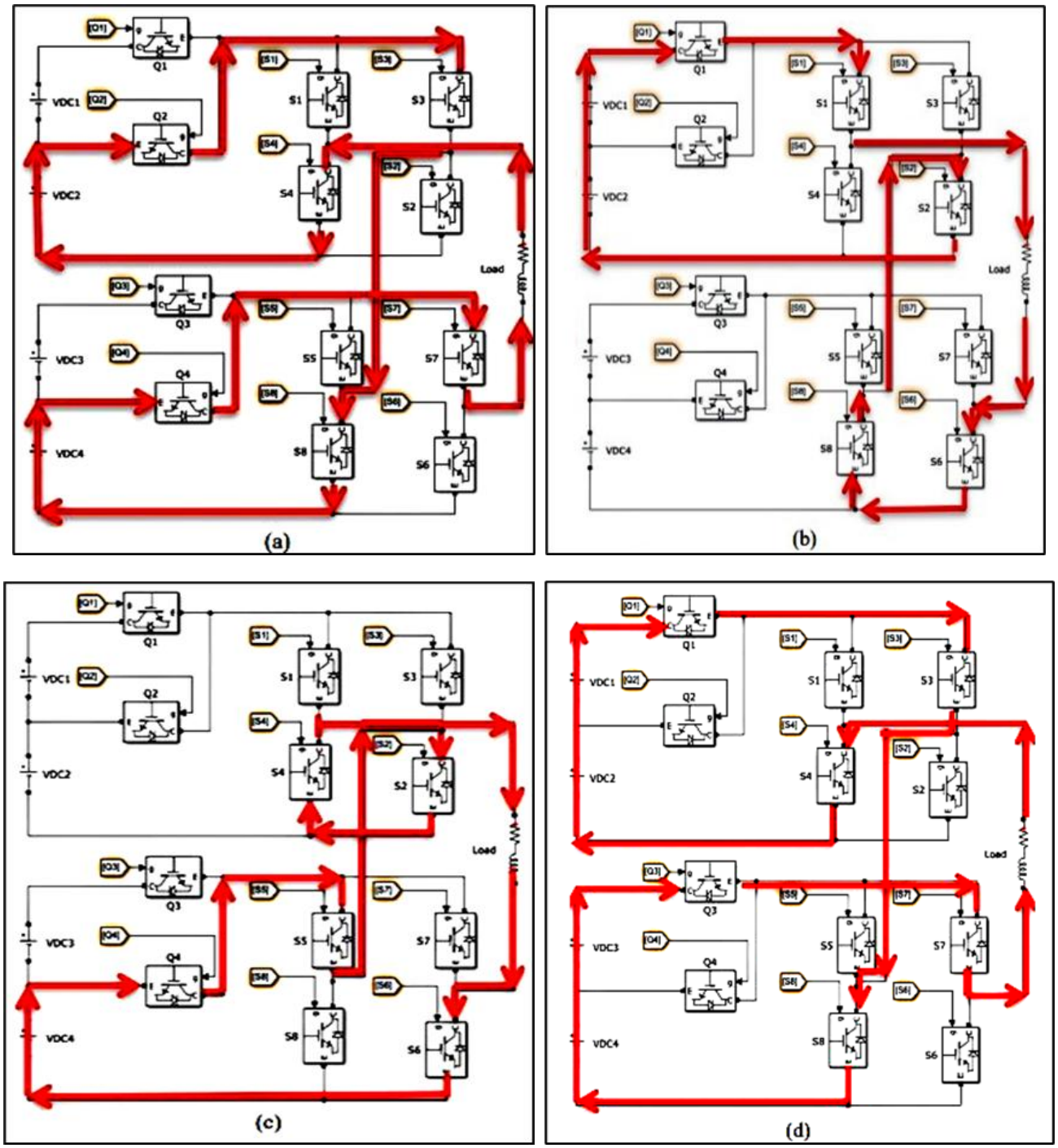

Fig. 9: Current path diagram in various operating modes at output voltage of (a) 12 V, (b) -6 V, (c) 5 V, (d) -12 V

The combination of these switching states enables both positive and negative polarity voltage levels, thereby achieving full-cycle operation. The proposed design thoughtfully incorporates four distinct DC voltage sources (130, 130, 26 & 26 V), utilizing a total of 12 switches to achieve an impressive 25-level output voltage range from +12 V_{dc} to -12V_{dc}. This innovative configuration offers significant benefits, including a 75% reduction in the number of switches and a 67% decrease in the number of DC sources. The arrangement of the DC voltage sources in thoughtfully organized in a ratio of 1: 1.5: 5 V_{dc}. For further clarification, Table. 1, provides the switching patterns of MLI needed to attain the desired 25-level output voltage. Fig. 9, depicts a comprehensive current route diagram for the inverter system's various modes of

operation. Fig. 9 (a), depicts the current route used to obtain an output voltage of +12 V_{dc}, which is especially important for specific applications. Fig. 9 (b), depicts the current route required to provide an output of +6 V_{dc}, a configuration that is frequently used in power supply applications that need a negative voltage reference. Fig. 9 (c) depicts the current route for producing a +5 V_{dc} output voltage, which is a commonly used standard for low-voltage electronic equipment. Finally, Fig. 9 (d) displays the current route required to obtain an output voltage of -12V_{dc}, which is frequently used in analog circuits and other specialized electronic applications. Careful gating signal design ensures that complementary switches do not conduct simultaneously, preventing shoot through conditions and enhancing system reliability. Additionally, the topology inherently supports bidirectional current flow, making it suitable for inductive loads such as motor drives. This makes the proposed configuration highly suitable for high-efficiency and high performance electric vehicle drive applications.

By assuming symmetric wave form with 25- level, RMS voltage is given by (18 – 19),

$$V_{RMS} = \sqrt{\frac{1}{T}\left(\int_0^T V_0^2(t)dt\right)} \quad (18)$$

$$V_{RMS} \approx \sqrt{\frac{1}{T}\left(\sum_{k=1}^{n}(V_k^2.\Delta t_k)\right)} \quad (19)$$

Where
$V_k = Voltage\ at\ each\ level$
$\Delta t_k = Duration\ of\ level\ k$
$\Delta t_k = Duration\ of\ level\ k$

Table. 1 presents the switching states for the proposed 25-level MLI topology and Fig. 10 and Fig. 11 depict the output voltage waveform and its FFT analysis for single phase 25 level MLI, respectively. To improve the performance and stability, numerous PWM approaches were carefully incorporated with multilayer inverters, resulting in a considerable reduction in total THD. This decrease is critical for ensuring the quality of power transmission and limiting potential interference with other electronics. Furthermore, it was tested on numerous multicarrier PWM systems for efficacy in a variety of settings. In this work, it was selected to use a MCPWM technique based on PD methodology. To optimize waveform morphologies and achieve lower THD levels in both output voltage and current, this approach is specially designed, resulting in improved overall system performance and efficiency. FFT analysis is an effective method for decomposing signals into their frequency components and applies to both 1-phase and 3-phase voltage signals. When it comes to 3-Phase signals, the analysis considers three distinct voltage waveforms.

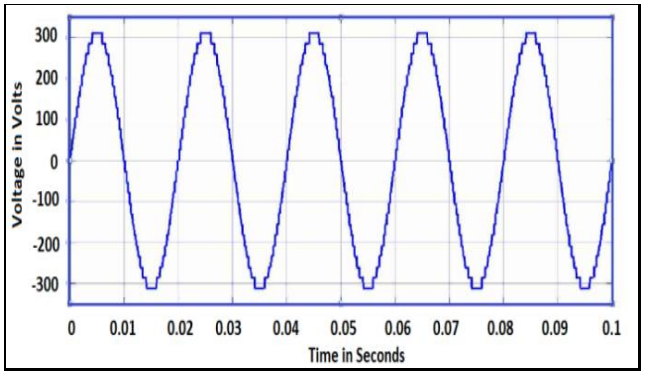

Fig. 10: Output voltage waveform of single phase 25-level MLI.

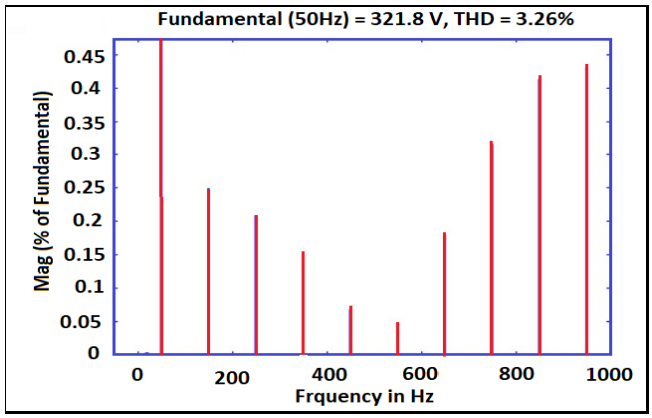

Fig. 11: FFT Analysis for single phase voltage.

6. Proposed 3-phase 25- level MLI configuration

The 3-phase 25-level MLI is a type of power converter used in HEVs to reduce THD improves the efficiency and enhance power quality. These inverters are designed to provide higher voltage levels with reduced switching losses making them ideal for EV applications. Fig. 12, represents the Matlab/Simulink model of proposed 3-phase 25-level MLI, and the output voltage of the 3-phases shown in the Fig. 13.

Table. 1: Switching states of 25-level output voltage

Conducting switches: 1 = ON, 0 = OFF													
Level	Q_1	Q_2	Q_3	Q_4	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{0ut}
1	1	0	1	0	1	1	0	0	1	1	0	0	$12V_{dc}$
2	0	1	1	0	1	1	0	0	1	1	0	0	$11V_{dc}$
3	0	0	1	0	0	1	0	1	1	1	0	0	$10V_{dc}$
4	0	1	1	0	0	0	1	1	1	1	0	0	$9V_{dc}$
5	1	0	1	0	0	0	1	1	1	1	0	0	$8V_{dc}$
6	1	0	0	1	1	1	0	0	1	1	0	0	$7V_{dc}$
7	0	1	0	1	1	1	0	0	1	1	0	0	$6V_{dc}$
8	0	0	0	1	0	1	0	1	1	1	0	0	$5V_{dc}$
9	0	1	0	1	0	0	1	1	1	1	0	0	$4V_{dc}$
10	1	0	0	1	0	0	1	1	1	1	0	0	$3V_{dc}$
11	1	0	0	0	1	1	0	0	0	1	0	1	$2V_{dc}$
12	0	1	0	0	1	1	0	0	0	1	0	1	$1V_{dc}$
13	0	0	0	0	1	1	1	0	1	0	1	0	0
14	0	1	0	0	0	0	1	1	1	0	1	0	$-1V_{dc}$
15	1	0	0	0	0	0	1	1	1	0	1	0	$-2V_{dc}$
16	1	0	0	1	1	1	0	0	0	0	1	1	$-3V_{dc}$
17	0	1	0	1	1	1	0	0	0	0	1	1	$-4V_{dc}$
18	0	0	0	1	1	0	1	0	0	0	1	1	$-5V_{dc}$
19	0	1	0	1	0	0	1	1	0	0	1	1	$-6V_{dc}$
20	1	0	0	1	0	0	1	1	0	0	1	1	$-7V_{dc}$
21	1	0	1	0	1	1	0	0	0	0	1	1	$-8V_{dc}$
22	0	1	1	0	1	1	0	0	0	0	1	1	$-9V_{dc}$
23	0	0	1	0	1	0	1	0	0	0	1	1	$-10V_{dc}$
24	0	1	1	0	0	0	1	1	0	0	1	1	$-11V_{dc}$
25	1	0	1	0	0	0	1	1	0	0	1	1	$-12V_{dc}$

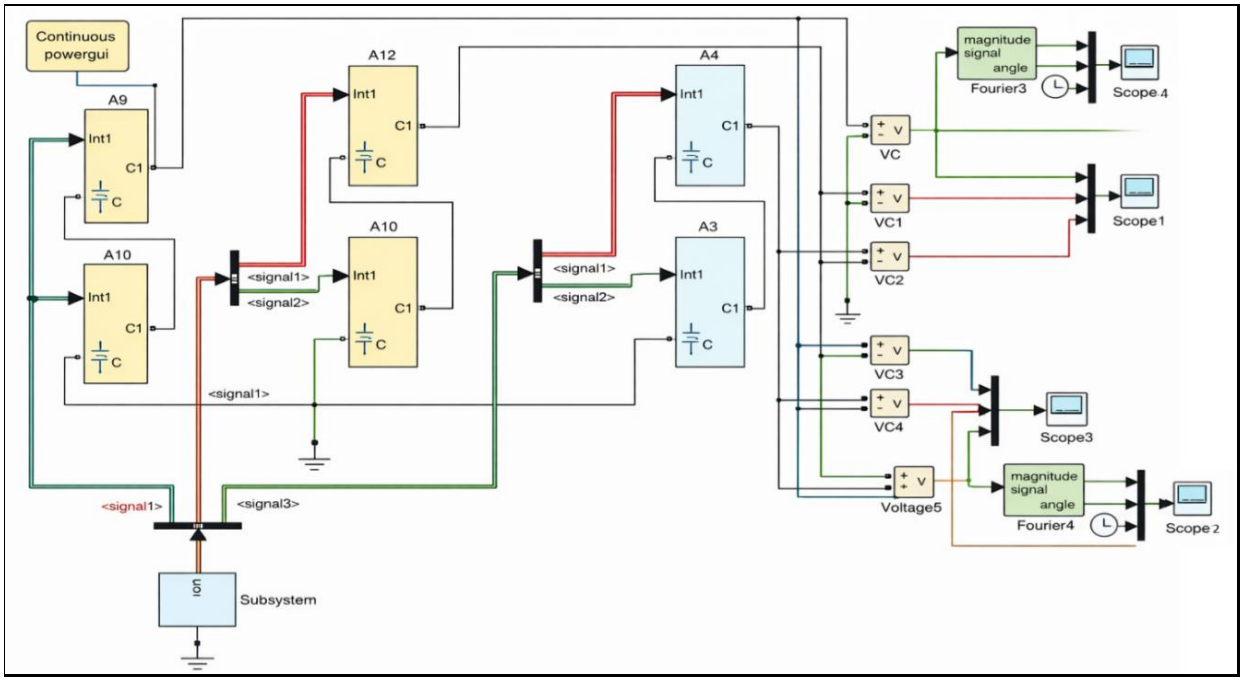

Fig. 12: Matlab/Simulink model of proposed 3-phase 25-level MLI.

Table. 2: Comparative analysis

Parameter	11-level MLI	17-level MLI	19-level MLI	21-level MLI	Proposed MLI
THD (%)	4 – 6	2.5 – 4	2.3 - 3.5	2-3.2	< 2.40
Efficiency (%)	94 – 96%	96 – 97.5%	96 – 97%	96 – 97%	97%+
Switching Loss	Less	Moderate	High	High	Less
Thermal Performance	Moderate	Good	Critical	Challenging	Good
Power Density	High	Very High	Very High	Ultra-High	Maximum
Control Complexity	Medium	High	High	Very High	Less

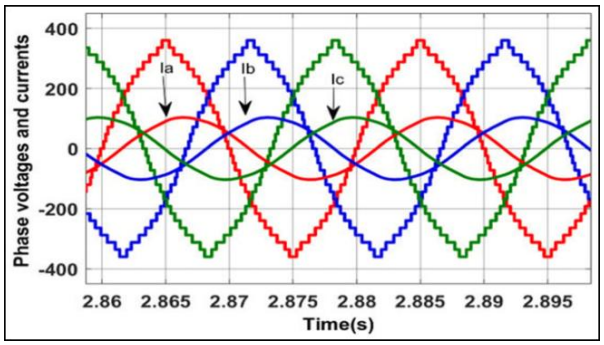

Fig. 13: Output waveforms of 3- phase MLI

FFT analysis is an effective method for decomposing signals into their frequency components and applies to both 1-phase and 3-phase voltage signals. When it comes to 3-Phase signals, the analysis considers three distinct voltage waveforms. This approach enables the identification of phase imbalances and harmonic distortion in the system, contributing to a more comprehensive understanding of its performance. Fig. 14, depicts the FFT analysis for the 3-phase output voltage of the proposed 25-level MLI. The comparative analysis among other conventional MLIs with the proposed 3-phase, 25-level MLI topology is provided in the Table. 2.

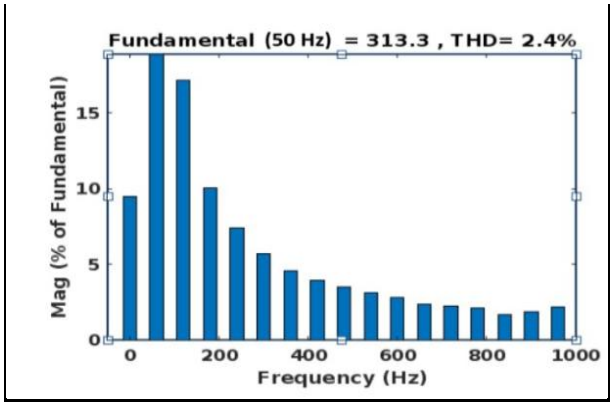

Fig. 14: FFT Analysis for 3-phase voltage

7. Conclusion

HEVs are emerging as a significant technology for both present and future generations. These vehicles are complex dynamic systems, with 3-phase inverters being utilized for high power applications. When engaging a voltage source inverter functioning in 120˚ conduction mode, harmonic losses and copper winding are minimized, ensuring accurate output waveforms for rotor speed, rotor angle and electromagnetic torque in both open loop and closed loop configurations. The comparative analysis with other conventional MLIs is provided in the Table. 2. Simulation results obtained using the Mat lab/Simulink environment demonstrate the effectiveness of this study. To summarize, the proposed 3-phase 25-level integrated inverter configuration offers a highly efficient and forward-thinking solution for HEVs. By carefully optimizing the number of switching components and DC-sources, this design effectively minimizes system complexity while maintaining superior output voltage quality with reduced THD. In this study, the proposed system has achieved a low THD of 2.4%. Furthermore, by using advanced multicarrier PWM techniques refines performance is refined, ensuring seamless transitions across voltage levels. Moving forward, future studies could focus on advancing modulation strategies and exploring system wide integration to improve scalability and adaptation across various electric vehicle platforms.

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Data Availability Statement

All data generated or analyzed during this study are included in this published article and its supplementary information files.

Conflict of Interest

The authors declared "No conflict of interest".

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Conceptualization, DT and AI; methodology, DT; software, DT; validation, DT and AI; formal analysis, AI; investigation, DT; resources, DT; data curation, DT; writing—original draft preparation, DT; writing—review and editing, AI; visualization, AI; supervision, AI; project administration, AI; funding acquisition, AI. All authors have read and agreed to the published version of the manuscript.

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